**Electronic Circuits**

**Two Marks questions and Answers**

1. **Why do we choose q point at the center of the load line? (Understand)**

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

# Name the two techniques used in the stability of the q point .explain. (Remember)

Stabilization technique: This refers to the use of resistive biasing circuit which allows IB to vary so as to keep IC relatively constant with variations in Ico and VBE.

Compensation techniques: This refers to the use of temperature sensitive devices such as thermistors diodes. They provide compensating voltages and currents to maintain operating point constant.

# Give the expression for stability factor. (Remember)

S = (1 + β) / 1 – β (  IB /  IC)

# List out the different types of biasing. (Remember)

Voltage divider bias, Base bias, Emitter feedback bias, Collector feedback bias

# What do you meant by thermal runway? (Remember)

Due to the self heating at the collector junction, the collector current rises.

This causes damage to the device. This phenomenon is called thermal runway.

# Why is the transistor called a current controlled device? (Understand)

The output characteristics of the transistor depend on the input current. So the transistor is called a current controlled device.

# Define current amplification factor? (Remember)

It is defined as the ratio of change in output current to the change in input current at constant other side voltage.

# What are the requirements for biasing circuits? (Understand)

The q point must be taken at the Centre of the active region of the output Characteristics.

* 1. Stabilize the collector current against the temperature variations.
	2. Make the q point independent of the transistor parameters.
	3. When the transistor is replaced, it must be of same type.

# When does a transistor act as a switch? (Understand)

The transistor acts as a switch when it is operated at either cutoff region or Saturation

region.

# What is the need for biasing in transistor amplifier. (Anna Univ May 2011) (Remember)

To use the transistor in any application it is necessary to provide sufficient Voltage and current to operate the transistor. This is called biasing.

# What is operating point?(or)q-point (Anna Univ Dec 2011) (Nov- Dec 2016) (May-June 2016)(Remember)

For the proper operation of the transistor a fixed level of current and Voltages are required. This values of currents and voltages defined at a point at which the transistor operate is called operating point.

# What is stability factor? (Anna Univ Dec 2011) (Remember)

Stability factor is defined as the rate of change of collector current with respect to the rate of change of reverse saturation current

# 11. Give the stability factor S for the fixed bias circuit. (Au may 2007) (Remember)

The stability factor for the fixed bias circuit is, S=1+β

# What is d.c load line? (Remember)

The d.c load line is defined as a line on the output characteristics of the transistor which gives the value of Ic & Vce corresponding to zero signal condition.

# What are the advantages of fixed bias circuit? (Remember)

This is simple circuit which uses a few components. The operating point can be fixed anywhere on the Centre of the active region

# Explain about the various regions in a transistor? (Remember)

The three regions are active region saturation region cutoff region.

# Explain about the characteristics of a transistor? (Remember)

Input characteristics: it is drawn between input voltage & input current while keeping output voltage as constant.

Output characteristics: It is drawn between the output voltage &output current while keeping input current as constant.

# What is the necessary of the coupling capacitor? (Remember)

It is used to block the dc signal to the transistor amplifier. It allows a c & blocks the d c.

# What is the disadvantage of collector bias? (Remember)

RL should be made very high to decrease the effect of changes in β affecting, IC much, which is not always practical. Also because of negative feedback, the efficiency is reduced.

# How does the thermistor compensation work? (Remember)

The thermistor has a negative temperature coefficient i.e., its resistance decreases with the increase in temperature. So any excess collector current is decreased because of the reduction in the active current through the device.

# Write a major difference between JFET and E-MOSFET biasing. (Understand)

Biasing circuits for E-MOSFET are similar to the circuit used for JFET biasing. The primary difference between the two is the fact that E-MOSFET only permits operating points with positive value of VGS for n channel and negative value of VGS for p channel.

# Why do you fix the operating point in the middle of the dc load line? (Understand)

The transistor act as a amplifier only in the active region. If the ac signal has to be amplified, then it is necessary that the transistor remains in the active region throughout the ac cycle. So, the operating point called as Q-point defined by a steady state VCE and IC is fixed in the middle of the dc load line.

# Explain one application JFET used as variable resistor. (Remember)

FET is operated in constant current position of its output characteristics. FET can also be used in the region before pinch-off where VDS is small. In this region it is used as voltage controlled resistor (or) voltage variable resistor (VVR). The VVR can be used to vary the voltage gain of a multistage amplifier. This action is called as Automatic Gain Control(AGC).

# What do you understand by DC & AC load line? (Nov- Dec 2016) (Understand) DC Load Line:

It is the line on the output characteristics of a transistor circuit which gives the values of Ic & Vce corresponding to zero signal (or) DC Conditions.

# AC Load Line:

This is the line on the output characteristics of a transistor circuit which gives the values of Ic & Vce when signal is applied.

# What is the function of Q-point? (Anna Univ Dec 2012) (Understand)

For the proper operation of the transistor a fixed level of current and Voltages are required. This values of currents and voltages defined at a point at which the transistor operate is called operating point.

# What is thermal stability? (Anna Univ Dec 2013) (Remember)

Due to the self heating at the collector junction, the collector current rises.

This causes damage to the device. This phenomenon is called thermal runway.

# What do u mean by punch through? (MAY JUNE 2014) (Remember)

On increasing the Reverse bias voltage then at a time instant the width of the base becomes zero and this effect is called punch through effect and that reverse bias voltage is called punch through voltage.

# What is thermal runaway? (MAY JUNE 2014) (Remember)

The problem with increasing temperature causing increasing collector current is that more current increase the power dissipated by the transistor which, in turn, increases its temperature. This self-reinforcing cycle is known as thermal run away, which may destroy the transistor.

# Find the collector and base current of circuit given hfe=100 , VBE=0.7 V (NOV/DEC 2014) (Understand)



1. **What are the operating regions of N-Channel MOSFET and how do you identify the operating region? (NOV/DEC 2014) (Remember)**

The operating regions of N-Channel MOSFET are cut-off region , sub threshold region or weak inversion region . The operation regions are identified based on the Q point.

# List out the importance of selecting the proper operating point ? (APRIL/MAY 2015) (Remember)

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

# Draw the DC load line of the circuit shown (APRIL/MAY 2015) (Remember)



1. **What is the impact of temperature on drain current of MOSFET? (Nov-Dec 2016) (Understand)**

The drain current depends on carrier mobility (which decreases with increasing temperature by about -0.3 %/deg C); carrier concentration (which increases negligible with temperature), and threshold voltage (which decrease with temperature by about -2 mV/deg. C).

At gate voltages just above the threshold voltage (say < 500 mV above), the threshold variation dominates, and drain current increases with temperature. Conversely, at significantly higher gate voltages (say more than 1 V above threshold), the mobility term dominates, and drain current decreases with temperature.

This is because, at all but very low drain currents, the temperature dependence is dominated by the negative temperature coefficient of the threshold voltage. This means that, as the device temperature increases, the current through the device decreases due to two competing mechanisms.

# Give the methods of biasing a JFET? (May-June 2016)(Remember)

The various biasing methods of FET are fixed bias, voltage divider bias , self bias

**Part – B**

* 1. For a collector to base bias circuit, show that : **(Remember)**

S = 1 + β/ 1 + β (RC / RC + RB)

* 1. For a self bias circuit, show that : **(Remember)**

S = 1 + β/ 1 + β (RE / RE + RB)

* 1. Draw the circuit diagram of self-bias circuit using CE configuration and explain how it stabilizes operating point. ( 8 marks) **(Understand)**
	2. Define 3 stability factors. Derive and explain the condition to avoid thermal runaway. ( 8m) **(Understand)**
	3. What is meant by bias stability? What factors affect BJT biasing? (8m) **(Remember)**
	4. With the help of a neat diagram explain the voltage divider biasing method for JFET.(8m) **(Remember)**
	5. Derive an expression for stability factor. ( 6 marks) **(Remember)**
	6. Describe the stability in fixed bias and self bias and compare their performance.(10m)

# (Remember)

* 1. Explain in detail the biasing of MOSFET. ( 8 marks) **(Remember)**
	2. Describe how AC and DC load lines are drawn. ( 8 marks) **(Understand)**
	3. Prove that self bias is better bias compared to collector to base bias.(8marks)

# (Anna Univ May 2005) (Understand)

* 1. Design a fixed bias circuit to have operating point of (10 V, 3 mA).The circuit is supplied with 20V and uses a silicon transistor of hfe = 250 (8 marks)**(AU- May 2005) (Create)**
	2. Prove that collector to base bias is better than fixed bias. ( 8 marks) **(Remember)**
	3. Why biasing is necessary in BJT amplifier and explain the concept of DC load line with neat diagram**(AU - Dec 2007) (Remember)**
	4. Draw and explain voltage divider biasing using FET and derive for its stability factor

# (Anna Univ May 2008) (Remember)

* 1. Determine the bias resistor Rb for fixed bias and collector to base bias and compare the stability factor S for both of them. Give Vcc=12V, RL=330Ω, IB=0.3mA,β=100, VCEq=6V**. (Anna Univ May 2007) (Create)**
	2. Draw self Bias and derive all stability factors ( 16 marks) **(Anna Univ Dec 2010) (Remember)**
	3. Locate the operating point of the circuit **(Anna Univ Dec 2010) (Remember)**
	4. Derive the expression of stability factor for collector feedback amplifier. (8m)**(AU May11) (Remember)**
1. Calculate operating point ( 8 marks) **(Anna Univ May 2011) (Remember)**
2. What is the need for bias compensation? Derive the method of bias compensation using diodes.( 9 marks) **(Anna Univ Dec 2011) (Remember)**
3. Explain the use of thermistor and sensistor for bias compensation. ( 7 m) **(Remember) (AU-Dec 2011)**
4. For a voltage divider bias circuit, calculate Vce and Ic, where β=100,R1=10k, R2=5k,Rc=1k and RE=500Ω, Vcc=10v. **(Au-may2012) (Create)**
5. Discuss the various techniques of stabilization of Q-point in transistor. **(Au-may2012) (Remember)**
6. Draw and explain voltage divider biasing and explain the method of drawing dc load line o the output characteristics **(Anna Univ Dec 2012) (Remember)**
7. Comment on fixed biasing circuit of BJT and FET. Explain the procedure for locating suitable operating point on the characteristics curve **(Anna Univ Dec 2013) (Understand)**
8. What is the need for bias compensation? Derive the method of bias compensation**(Anna Univ may 2013) (Remember)**
9. Briefly describe about any two bias compensation technique of BJT **(MAY JUNE 2014) (May June 2016)(Remember)**
10. with neat circuit diagram and needed expressions explain the working principle of self bias of transistor **(MAY JUNE 2014) (Remember)**

31 . what is stability? What is the need for load line and quiescent point calculation?

# (MAY JUNE 2014) (Remember)

1. Calculate the operating point of the self biased JFET having the supply voltage VDD=20V, maximum value of drain current IDSS=10mA and VGS=-3V at ID =4 mA. Also determine the values of resistors RD and RS to obtain the bias condition **(MAY JUNE 2014) (Analyze)**
2. Design Emitter bias for BJT with IC=2mA, VCC=18V ,VCB= 10 V and β=150

# (NOV/DEC2014) (Create)

1. Derive the stability factor of self bias circuit of BJT. **(NOV/DEC2014) (Remember)**
2. Design voltage divider bias circuit for NMOS , such that IDQ =400µA ,VDD=14 V, VDS=2.3V , kn=µnCux (W/L) = 1ma/V2 ,Vt=1V . Assume a current of 1 µA through R1 and R2 and Vs=1.2 V **(NOV/DEC2014) (Create)**
3. The parameter for each transistor in the circuit are hfe=100 and VBEon=0.7 V. Determine the Q-Point values of base , collector and emitter current in Q1 and Q2. **(APRIL/MAY 2015) (Analyze)**



1. Analyze a BJT with a voltage divider bias circuit , and determine the change in the Q point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be RB1 = 56 kΩ, RB2 = 12.2 kΩ , Rc = 2 kΩ , RE = 0.4 kΩ Vcc = 10V VBE(on)=0.7V and β=100. (**Nov- Dec 2016)(Analyze)**
2. Consider the circuit shown below with transistor parameters IDSS=12 mA, VP = -4V , and λ= 0.008 V-1 . Determine the small signal voltage gain Av = Vo / Vi (**Nov- Dec 2016) (Create)**



Design the circuit given below such that IDQ = 100 μA , VSDQ =3V , and VRS=0.8 V. Now that VRS is the voltage across the source resistor RS . The value of the larger bias resistor either R1 and R2 is to be 200 kΩ. Transistor parameter values are KP=100μA/V2 and VTP = -

1.4 V. The conduction parameter, KP may vary by ± 5 percent. (**Nov- Dec 2016) (Create)**



1. Compare the various biasing methods using BJT in terms of its stability factors**?(May-June 2016)(Remember)**

# ASSIGNMENT QUESTION

* 1. Design a fixed bias circuit Vcc=12V, Vc=6V, Ib=40µA, β=80 (**Create)**
	2. An NPN transistor if β=50 is used in CE circuit with Vcc=10V and Rc=2K. the bias is obtained by connecting 100K resistor from collector to base. Find Q point and Justify the system is Stable or not . (**Analyse)**
	3. Find Q –point Vcc=10V, β=50, Rc=1K, RE=1000,Rb=200K **(Apply)**
	4. Design IcQ=1mA and VCeQ=6V.Assume Vcc=10V, β=100 and Vbe (on)=0.7V

# (Create)

# Part A

1. **What is an amplifier? (Anna Univ May 2010) (Remember)**

An amplifier is a device which produces a large electrical output of similar characteristics to that of the input parameters.

# How are amplifiers classified according to the input? (Remember)

* 1. Small signal amplifier 2. Large signal amplifier

# How are amplifiers classified according to the transistor configuration? (Remember)

* 1. Common emitter amplifier 2. Common base amplifier
1. Common collector amplifier

# What is the different analysis available to analyze a transistor? (Remember)

* 1. AC analysis 2. DC analysis

# How can a DC equivalent circuit of an amplifier be obtained? (Understand)

By open circuiting the capacitor.

# How can a AC equivalent circuit of a amplifier be obtained? (Understand)

By replacing dc supply by a ground and short- circuiting capacitors.

# What is feed back? (Remember)

It is the process of injecting some energy from the output and then returns it back to the

input.

# What are feedback amplifiers? (Remember)

An amplifier which uses feedback principle is called as feedback amplifiers.

# What are the types of feed back? (Remember)

* 1. Positive feedback 2. Negative feedback.

# What is positive feedback? (Remember)

If the feedback signal is applied in such a way that it is in phase with the input signal and thus increases it is said to be positive feedback.

# What is negative feedback? (Remember)

If the feedback signal is applied in such a way that it is out of phase with the input signal and thus decreases it is said to be positive feedback.

# Which feedback decreases the gain of the amplifier? (Remember)

Negative feed back

# Which feedback increases the gain of the amplifier? (Remember)

Positive feedback

What is the advantage of negative feedback? (Remember)

* 1. Increased stability 2. Increased bandwidth

3. Decreased noise 4. Less frequency distortion

# Define sensitivity. (Remember)

It is the ratio of percentage change in voltage gain with feedback to the percentage change in voltage gain without feedback.

# Define Desensitivity. . (Anna Univ May 2010) (Remember)

It is the ratio of percentage change in voltage gain without feedback to the percentage change in voltage gain with feedback. the reciprocal of sensitivity.

# What is an op-amp? (Remember)

The operational amplifier is a multi-terminal device, which is quite complex internally. An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package. It is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions.

# What are the characteristics of ideal op-amp? (Remember)

1. Open loop voltage gain, (AOL) =α .
2. Input impedance (Ri) =α.
3. Output impedance (Ro) = 0
4. Bandwidth (BW) =α.
5. Zero offset Vo = 0, when V1 = V2 = 0

# Define loading? (Anna Univ May 2011) (Remember)

A large value of Rc cannot be used in a circuit since, a large value of resistance requires a large chip area. For large Rc, quiescent drop across it increases and hence a large power supply is required.

These difficulties removed by using a current source. Hence, a current source can also be used as an active load for an amplifier to obtain a very large voltage gain.

# Define the four h-parameters. (Au may 2007) (Remember)

The dimensions of the hybrid parameters are not alike, that is they are hybrid in nature so they are called hybrid parameters.

h11 = [ V1/I1] at V2=0; h11 = Input impedance with output port short circuited. h12 = [ V1/V2] at I1=0; h12 = Reverse voltage gain with input port open circuited. h21 = [ I2/I1] at V2=0; h11 = Forward current gain with output port short circuited. h22 = [ I2/V2] at I1=0; h11 = output impedance with input port open circuited.

# What is CMRR? Derive its expression. . (Au may 2007) (Remember)



1. **State Millers theorem(Anna Univ May 2008) (Remember)**



1. **Draw darlington amplifier with Bootstrapp arrangement. (AU- Dec 2010) (Remember)**



1. **What are the salient features of hybrid parameters? (Remember)**

The salient features of hybrid parameters are,

1. h parameters are real numbers,
2. They are easy to measure.
3. They are convenient to use in circuit analysis and design
4. Easily convertible from one configuration to other
5. Readily supplied by manufactures.

# Write the input impedance, output impedance, voltage gain and current gain of the common emitter amplifier in terms of h parameters for the fixed bias condition? (Remember)

Current gain Ai = -hfe

Voltage gain Av = (hfeRC)/hie Input Impedance Zi = hie Output Impedance Zo = RL ||RC

# Define Miller effect in input capacitance? (Anna Univ May 2013) (Remember)

For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device.

CMi = (1-Av)Cf ; CMo=Cf

Cf = Inter electrode capacitance between input and output.

# What does bootstrapping mean? (Anna Univ May 2012) (Understand)

In Darlington transistor pair circuits, the input impedance is reduced because of the biasing resistors in the circuit. To overcome this, decrease in the input resistance due to the biasing network, a small capacitor and resistance R3 are added in the circuit. This improved the input impedance of the darlington pair circuit.

C is added at the input side and R3 is connected between output and input circuits. Reff = Effective input resistance.

Reff = R3/(1-Av)

Reff = Large value Av= Voltage gain.

# Why we go for differential amplifier? (or) What is the need of differential amplifier? (Anna Univ dec 2013) (Remember)

The need for differential amplifier arises in many physical measurements, in medical electronics and in direct coupled amplifier applications. In this amplifier, there will be no output voltage resulting from thermal drifts or any other changes provided; changes in both halves of the circuits are equal.

# Why should a differential amplifier have a high CMRR? (Anna Univ dec 2013) (Remember)

A high CMRR means a low common mode gain. We know that most of the common mode signals are just noise pickups. So to get a high fidelity signal output CMRR should be high.

# What is darlington connection? (MAY JUNE 2014) (Remember)

In electronics, the Darlington transistor (often called a Darlington pair) is a compound structure consisting of two bipolar transistors (either integrated or separated

devices) connected in such a way that the current amplified by the first transistor is amplified

further by the second one.

# Write about the characteristic of common emitter amplifier? (MAY JUNE 2014) (Remember)

The voltage gain of the common emitter amplifier is medium

The current gain of the common emitter transistor amplifier is medium The power gain of the common emitter amplifier circuit is high Input/Output is having a phase relationship of 180 degrees

Input and output resistance of common emitter amplifier are medium

# Draw the AC equivalent circuit of figure given below (NOV/DEC2014) (Remember)



1. **Find CMRR of differential amplifier with differential gain of 300 and common mode gain of 0.2 ? (NOV/DEC2014) (Understand)**



1. **Define CMRR of BJT Differential amplifier. How to improve it.? (APRIL/MAY 2015) (Remember)**



A high CMRR means a low common mode gain. We know that most of the common mode signals are just noise pickups. So to get a high fidelity signal output CMRR should be high.

CMRR = −gm RE

By increasing the value of RE , the CMRR will increase, in other words the performance of the differential amplifier can be improved by simply increasing the emitter resistance. A common practice is to use a current source to replace RE , the results will be high CMRR

# A small signal source Vi(t) = 20cos20 t + 30 sin 106t is applied to a transistor amplifier as shown in figure below. The transistor has hfe=150, r0=∞ and rπ= 3kΩ . determine Vo(t). (APRIL/MAY 2015) (Apply)



1. **Draw the small signal AC equivalent circuit of the BJT? (Nov-Dec 2016) (Remember)**



1. **What is the need of load line? (May-June 2016)(understand)**

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

# Draw thew cascade amplifier and its equivalent circuit? (Remember)(May-June 2016)



**Part – B**

* 1. Derive the expression for AI, AV, Ri and Ro for CE amplifier using h-parameter model.

(10 marks) **(Remember)**

* 1. Explain with circuit diagram the boot strapped Darlington emitter follower. Derive the expression for its input impedance**. (Anna Univ Dec 2005) (Remember)**
	2. Derive the expressions for current gain, voltage gain, input impedance and output impedance for an emitter follower circuit. ( 10 marks) **(Remember)**
	3. Derive the expression for the voltage gain of common collector amplifier. **(Remember)**
	4. Draw a small signal low frequency model for an FET and explain. (6 marks)

# (Remember)

* 1. Derive the expression for the voltage gain of **(Remember)**
		1. Common source amplifier
		2. Common drain amplifier configurations, under small signal low frequency conditions.
	2. Derive the expression for the voltage gain of: common drain amplifier configurations, under small signal low frequency conditions.( 8 marks) **(Remember)**
	3. What is cascode amplifier? Explain. ( 8 marks) **(Remember)**
	4. Draw a two stage RC coupled amplifier and explain the need for each component used. If the current gain of each stage is A1, what is the overall current gain? **(Understand)**
	5. Draw a cascode amplifier and derive the expression for the four important parameters AV, AI, Zi and Zo. **(Remember)**
	6. Draw a two stage RC coupled amplifier of identical stages and derive the expressions for its overall voltage gain and current gain, if the individual stage gains are A and A, respectively. Assume ideal source. **(Remember)**
	7. Draw the circuit diagram for a differential amplifier using BJTs. Describe common mode and differential modes of working. ( 8 marks) **(Remember)**
	8. Discuss in detail how the current gain, input impedance, Voltage gain and output impedance of a transistor amplifier can be obtained using h-Parameters.**(Anna Univ May 2007) (Remember)**
	9. Discuss the operation of emitter coupled differential amplifier **(Au Dec 2007/may 2012) (Remember)**
	10. Write the improving methods of CMRR **(Anna Univ Dec 2007) (Remember)**
	11. Explain the operation of basic emitter coupled differential amplifier and derive its CMRR

# (Anna Univ May 2008) (Remember)

* 1. How does the constant current source increase the gain and hence CMRR in a differential amplifier. **(Anna Univ May 2008) (Understand)**
	2. Draw the hybrid model of CE amplifier and obtain its gain, input impedance and output impedance. Compare the performance of this CE amplifier with CC and CB configuration. **(Anna Univ May 2008) (Remember)**
1. Draw the differential amplifier and its ac equivalent circuit. Derive for Ad and Ac. (16marks) **(Anna Univ Dec 2010) (Remember)**
2. Describe the method to increase the input resistanse using Darlington connection. **(Anna Univ May 2011/2012) (Remember) (May June 2016)**
3. Draw the small signal equivalent model of CE amplifier circuit and analyze the circuit to obtain its gain,input and output impedance.(16 marks) **(Anna Univ Dec 2011) (Remember)**
4. Explain the effect of removing the bypass capacitor from the emitter resistance for CE amplifier circuit. (8 marks) **(Anna Univ Dec 2011) (Remember)**
5. Draw the circuit of emitter coupled differential amplifier and explain its operation. Analyze the circuit and obtain its transfer characteristics(16 marks) **(AU Dec 2011) (Remember)**

# Compare CB,CE and CC amplifiers. (Au-may2012) (Understand)

1. Draw the circuit of CE amplifier with coupling and bypass capacitors.with the help of equivalent circuits,obtain the equation of voltage gain inputand output impedance) **(Anna Univ Dec 2013) (Remember)**
2. Draw the circuit of emitter coupled BJT differential amplifier and explain the operation of the circuit) **(Anna Univ Dec 2013) (Remember)**
3. With neat diagram , analyze the transistor amplifier using h-parameter. **(MAY JUNE 2014)(Analyze)**
4. Describe with neat circuit diagram , the operation of common drain amplifier with small signal equivalent circuit. Derive the equation for voltage gain , input impedance and output amplifier. **(MAY JUNE 2014) (Remember)**
5. What is differential amplifier. **(MAY JUNE 2014) (Remember)**
6. Derive CMRR of differential amplifier with its equivalent circuit**. (NOV/DEC 2014) (Remember)**
7. explain the operation of cascade amplifier and derive gain, input and output impedance.

# (NOV/DEC 2014)(Understand)

1. Analyze a basic common base amplifier circuit and derive the expressions for its small- signal voltage gain , current gain , input impedance and output impedance.**(Nov- Dec 2016)(Analyze)**
2. With neat diagrams explain the operation and advantages of Darlington pair circuit . Also analyze its small-signal voltage gain and input impedance. .**(Nov- Dec 2016) (Analyze)**
3. What are the advantages and disadvantages of bridge rectifier circuit? (6 marks) **(Remember)**
4. With a capacitor filter, explain the working of a half wave rectifier and obtain its ripple factor. Compare it with π filter instead of capacitor filter. (10 marks) **(Remember)**
5. A half wave rectifier circuit is supplied from 230, 50Hz supply with a step down ratio of 3:1 to resistive load of 10KΩ. The diode forward resistance is 75Ω while transformer secondary resistance is 10Ω. Calculate the maximum, average, RMS value of current, d.c. output voltage, rectification efficiency and ripple factor. Derive the formula used.

# (Create)

1. Derive the expression for ripple factor FWR with π section filter. **(Anna Univ Dec 2007) (Remember)**
2. Derive the expression of ripple factor for the following filters: C, L, LC and π. FW rectified signal is applied as input. **(Remember)**
3. Describe the working principle of full wave rectifier and derive the expression for the ripple factor, rectifier efficiency VDC, IRMS, IDC and VRMS. With a neat diagram explain the operation of transistorized series type voltage regulator. **(Understand)**

(8 marks)

1. Explain with diagrams, how SCR can be used as variable full wave rectifier. (8 marks)

# (Remember)

1. Explain the function of switching regulators. (8 marks) **(Remember)**
2. Derive the ripple factor for FWR with capacitor filter (**Anna Univ May 2008) (Remember)**
3. Design the cascade circuit shown below to meet the following specifications VCE1= VCE2= 2.5V , VBE= 0.7 V , IC1=IC2= 1mA , and IR1=IR2=IR3=0.10 mA.



1. What are the changes in the AC characteristic of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are introduced in the design? Explain with necessary equations? **(May-June 2016 Remember)**
2. Calculate the small signal voltage gain of an emitter follower circuit given β=100 VBE(ON)

= 0.7 V ,VA =80 V ,ICQ = 0.793 mA ,VCEQ=3.4 V **(May-June 2016 )(Apply)**

# ASSIGNMENT QUESTION

1. Find input and output impedance, voltage and current gain for CB, RE=4K, Rc=3K. Assume Vbe=0.6V. **(Apply)**
2. If CMRR of an amplifier is 100dB Calculate Common mode gain, if differential gain is 1000. **(Apply)**
3. Design a CB amplifier Rs=1200Ω and the load impedance is =1000Ω, use suitable h- parameters**.(Create)**
4. Calculate the current gain ,voltage gain and power gain of CE and CB amplifier with load of 3KΩ and justify which amplifier gain is more than the other **(Analyse)**

# Part A

1. **Define input offset voltage? (Remember)**

It is defined as the voltage that must be applied between the input terminals of an op-amp to nullify the output.

# Define input offset current? (Remember)

It is defined as the algebraic difference between the current entering the inverting and non-inverting terminal of an op-amp.

# Define input bias current? (Remember)

It is defined as the average of the currents entering into the input terminals of an op-amp.

# What are the two compensating techniques used in frequency compensation? (Remember)

Two types of compensating techniques are used, they are,

a. External compensation b. Internal compensation

# What is compensated op-amp? (Remember)

Op-amp, which uses a capacitor internally for compensation, is called a compensated Op-amp. This op-amp has a high gain stability and low bandwidth.

# What are the methods used in external compensation technique? (Remember)

a. Dominant-pole compensation b. Pole-zero compensation

# Define slew rate? (Remember)

Slew rate can be defined as the maximum rate of change of output voltage of op-amp with respect to time.

# How can the slew rate be made faster? (Remember)

The slew rate can be made faster by having a high charging current or a small capacitance

value.

# What are the methods to improve slew rate? (Remember)

* 1. The slew rate can be improved with higher closed-loop gain and dc supply voltage. But the slew rate also varies with temperature. i.e., slew rate decreases with

increase in temperature.

* 1. Another method for improving slew rate is, the rate at which voltage across the capacitor increases is gain by, dVc/dt = I / C. where, I is the maximum current furnished by the op-amp to the capacitor

# What is a single stage transistor amplifier? (Remember)

When only one transistor with its associated circuitry is used to increase the strength of a weak signal, the complete circuit or network is known as single stage transistor amplifier.

# Why are hybrid parameters called so? (Remember)

Hybrid or h parameters are called so because they have mixed dimensions, one in ohms, another in mho and the remaining two are unitless.

# What do you understand by hybrid parameters? Mention their dimensions.(Understand)

The hybrid parameters are obtained by applying Thevenin’s theorem to the input and Norton’s theorem to the output port. These have mixed dimensions as shown below.

hi = input impedance in ohms hr = reverse voltages gain

ho = output admittance in mho hf = forward current gain

# What are the limitations of h parameters? (Remember)

1. It is very difficult if not impossible to get accurate values of h parameters for a transistor. The reason is that the h parameters are subject to variations due to temperature, operating point and from unit to unit.
2. A transistor behaves as a two port network for small signals only, hence h parameters can be used to analyze only the small signal (i.e., single stage) amplifiers.

# What is phase reversal? Explain with respect to amplifier? (Anna Univ May 2012) (Remember)

Phase reversal is the operation of obtaining an output which is 180˚ out of phase from the input signal. For example the output of CE amplifier is out of phase with the input. Cascading two amplifiers eliminates the phase reversal.

# What are the applications of CC and CE amplifiers? (Anna Univ May 2011) (Remember)

1. The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load.
2. Of the three configurations CE amplifier alone is capable of providing both voltage gain and current gain. Further the input impedance Zi and the output impedance Zo are moderately high. Hence CE amplifier is widely used for amplification purpose.

# Mention some methods of achieving drift compensation, in a differential amplifier. (Remember)

Though the symmetrical construction is supposed to ensure a low drift, some special circuitry like current mirror, diode, zener constant current source, etc., may be used for drift compensation.

# Why should a differential amplifier have a high CMRR?(Understand)

A high CMRR means a low common mode gain. We know that most of the common mode signals are just noise pickups. So to get a high fidelity signal output CMRR should be high.

# What is the disadvantage of a MOSFET input stage? (Anna Univ May 2012) (Remember)

The main disadvantage of using MOSFETs in the input stage is very low voltage gain due to low transfer conductance of the MOSFETs. So booster stages are required subsequently.

# Give the equation of overall upper and lower cut off frequency of multistage amplifier (Anna Univ May 2013) (Remember)

fL(n) = f L / ((21/n-1))

Where f L(n) – lower 3 dB frequency of identical cascaded stages n - Number of stages

fH(n) = f H ((21/n-1))

Where f H(n) – lower 3 dB frequency of identical cascaded stages n - Number of stages

# What do u mean by rise time? (MAY JUNE 2014) (Remember)

The [rise time,](https://en.wikipedia.org/wiki/Rise_time) tr, of an amplifier is the time taken for the output to change from 10% to 90% of its final level when driven by a [step input](https://en.wikipedia.org/wiki/Step_response). For a [Gaussian](https://en.wikipedia.org/wiki/Gaussian) response system (or a simple RC [roll off](https://en.wikipedia.org/wiki/Roll-off)), the rise time is approximated by:

tr \* BW = 0.35, where tr is rise time in [seconds](https://en.wikipedia.org/wiki/Second) and BW is bandwidth in [Hz](https://en.wikipedia.org/wiki/Hertz).

# State miller’s theorem ? (MAY JUNE 2014) (Remember)

The Miller's theorem establishes that in a linear circuit, if there exists a branch with impedance Z, connecting two nodes with nodal voltages V1and V2, we can replace this branch by two branches connecting the corresponding nodes to ground by impedances respectively Z / (1-K) and KZ / (K-1), where K = V2 / V1.

# Draw small signal model of JFET. (NOV/DEC2014) (Remember)



1. **What are the features of BiMOS cascade amplifier. (NOV/DEC2014) (Remember)**

A cascade amplifier is any [two-port network](https://en.wikipedia.org/wiki/Two-port_network) constructed from a series of amplifiers, where each amplifier sends its output to the input of the next amplifier in a [daisy chain](https://en.wikipedia.org/wiki/Daisy_chain_%28electrical_engineering%29).

The complication in calculating the gain of cascaded stages is the non-ideal coupling between stages due to loading. Two cascaded common emitter stages are shown. Because the input resistance of the second stage forms a [voltage divider](https://en.wikipedia.org/wiki/Voltage_divider) with the output resistance of the first stage, the total gain is not the product of the individual (separated) stages.

# Compare JFET and MOSFET amplifiers. (APRIL/MAY 2015)(Understand)

JFETs can only be operated in the [depletion mode](http://www.circuitstoday.com/demosfet-depletion-enhancement-mosfet) whereas MOSFETs can be operated in either depletion or in [enhancement mode.](http://www.circuitstoday.com/emosfet-enhancement-mosfet) In a JFET, if the gate is forward biased, excess- carrier injunction occurs and the gate current is substantial. Thus channel conductance is enhanced to some degree due to excess carriers but the device is never operated with gate forward biased because gate current is undesirable.

MOSFETs have input impedance much higher than that of JFETs. This is due to negligibly small leakage current.

JFETs have characteristic curves more flat than those of MOSFETs indicating a higher drain resistance.

When JFET is operated with a reverse bias on the junction, the gate current IG is larger than it would be in a comparable MOSFET. The current caused by minority carrier extraction across a reverse-biased junction is greater, per unit area, than the leakage current that is supported by the oxide layer in a MOSFET. Thus MOSFET devices are more useful in electrometer applications than are the JFETs.

# Find the unity gain bandwidth of MOSFET where gm=6mA/V ,Cgs=8 pF, Cgd= 4pF and Cds=1pF. (APRIL/MAY 2015)

1. **What is the impact of including the source resistance in the FET amplifier? (Nov- Dec 2016) (Understand)**

In the source resistor (SR) configuration, the ac input is applied at CG, the ac output is taken at CD and CS is omitted. This is analogous to the emitter-resistor configuration of the BJT.

# Why multi-stage amplifiers are required? (Nov- Dec 2016) (Understand)

In a multistage amplifier the output of one stage makes the input of the next stage. Normally a network is used between two stages so that a minimum loss of voltage occurs when the signal passes through this network to the next stage.

# What is body effect of MOSFET? How does it change the small signal equivalent circuit of MOSFET? (May June 2016) (Understand)

The threshold voltage of a MOSFET is affected by the voltage which is applied to the back contact. The voltage difference between the source and the bulk, VBS changes the width of the depletion layer and therefore also the voltage across the oxide due to the change of the charge in the depletion region. This results in a difference in threshold voltage which equals the difference in charge in the depletion region divided by the oxide capacitance

# Give the general conditions under which common source amplifier could be used? (May June 2016) (Understand)

One advantage of this is that the input is at zero dc volts such that the signal can be connected directly without interfering with the bias. The dc circuit equation for setting up the bias.

**Part – B**

* 1. Derive the expression for the CE short circuit current gain of transistor at high frequency.

# (Remember)

* 1. What are the effects of coupling and bypass capacitors on the bandwidth of the amplifier?

**(Remember)** ( 6 marks)

* 1. Derive the equation for gm which gives the relation between gm, IC and temperature.

**(Remember)** ( 8 marks)

* 1. Derive the expression for CE short circuit current gain and current gain with resistive load, at high frequencies. **(Apply)**
	2. Draw the high frequency hybrid π model for a transistor in the CE configuration and explain the significance of each component. **(Anna Univ May 2007)(Understand)**
	3. Define alpha cutoff frequency. (4marks) **(Remember)**
	4. What is the effect of Cb’c on the input circuit of a BJT amplifier at high frequencies? (10m) **(Remember)**
	5. Derive expression for the short circuit current gain of common emitter amplifier at HF. Define alpha cutoff frequency, beta cutoff frequency and transition frequency and derive their values in terms of the circuit parameters. **(Anna Univ May 2005)(Analyze)**
	6. Discuss the low and high frequency response of an amplifier. **(Anna Univ May 2007) (Remember)**
	7. Derive for upper and lower cut- off frequency of RC coupled BJT amplifier. Derive for upper and lower cut- off frequency of RC coupled BJT amplifier. **(AU May 2008) (Remember)**
	8. Draw high frequency equivalent circuit for FET amplifier and derive the value of all the parameters **(Anna Univ May 2008/may 2012) (Analyze)**
	9. Draw the high frequency hybrid π model for a transistor in the CE configuration and derive for higher cut-off frequency (12 marks)**(Anna Univ Dec 2010) (Remember)**
	10. With the help of high frequency π model of transistor, analyze the current gain of CE transistor amplifier with a short circuit load and obtain its gain frequency response (16 marks)**(Anna Univ May 2010/may 2012) (Analyze)**
	11. Draw and explain the high frequency equivalent circuit of a FET (8 marks)**( May 2010) (Remember)**
	12. Explain the effect of cascading transistor stages on the bandwidth of a cascaded amplifier (8 marks)**(Anna Univ May 2010) (Remember)**
	13. Draw the small signal hybrid model of CE amplifiers and derive the expression (16**)(Anna Univ Dec 2013) (Remember)**

#  Derive the needed expressions for high frequency π model for a transistor with neat circuit diagram. (MAY JUNE 2014) (Remember)

* 1. With the help of high frequency model of FET, Derive the necessary expressions for gain and bandwidth. **(MAY JUNE 2014) (Remember)**
	2. Derive gain, input and output impedance of common source JFET amplifier with neat circuit diagram and equivalent circuit. **(NOV/DEC 2014) (Remember)**
	3. Derive gain, input and output impedance of MOSFET source follower with neat circuit diagram and equivalent circuit. **(NOV/DEC 2014) (Remember)**
	4. Determine the Small-Signal voltage gain of a multistage cascade circuit shown in the figure below. The transistor parameters are Kn1 = 0.5mA/V2 , Kn2 = 0.2 mA/V2 ,VTN1=

VTN2 = 1.2 V and λ1 = λ2 = 0. The quiescent drain currents are ID1=0.2 mA and ID2=0.5 mA. . **(NOV/DEC 2016) (Apply)**



* 1. Draw the circuit of a basic common source amplifier with voltage divider bias and derive the expressions for voltage gain , input impedance and output impedance using small – signal model. (8). **(NOV/DEC 2016) (Remember)**
	2. Determine the voltage gain of the circuit , assuming the following parameters. VDD=3.3V , RD=10 kΩ , RG1= 140 kΩ , RG2=60 kΩ and Rsi= 4kΩ . The transistor parameters are VTN = 0.4V , Kn = 0.5mA/V2 , and λ= 0.02 V-2 (5) **(NOV/DEC 2016) (Apply)**
	3. Design a JFET source follower circuit with specified small signal voltage gain given IDSS

=12 mA , VP =-4V, λ=0.01V-1 . where RG=50K Supply is ± 10 Determine RS and IDQ

.such that the small signal voltage gain is at least AV= Vo/Vi =0.90 **(Create)(May June 2016)**

* 1. Determine the small signal voltage gain of a common source circuit containing a source resistor. The transistor parameter are VTN =0.8V , Kn=1mA/V2 and λ=0 with R1=11.5K RD=7K Rs=0.5K R2=35K **(Apply)(May June 2016)**

# ASSIGNMENT QUESTION

* + 1. For the given network i) determine fr ii) Sketch whether it is symptotes or Asymptotes iii) Locate the 3-db point iv)draw the actual frequency response curve **(Understand)**



* + 1. The rise time of certain amplifier is 10ns. Calculate B.W of the amplifier

# (Remember)

* + 1. Explain and Design Video amplifier to amplify the frequency range of 30Hz to 5.5MHz **(Create)**

# Part A

1. **What is a large signal amplifier? (Remember)**

A power amplifier does not amplify the power, but it draws dc power from supply and converts it into useful ac signal power at the output.

# What are the characteristics of a power amplifier? (Remember)

The characteristics which establish the amplifier as power amplifier are

* 1. Thick base i.e., smaller value of β
	2. Larger size of transistor – Ic is more ( > 100 mA)
	3. Collector load resistance Rc
	4. Transformer coupling

# What are the special characteristics of power transistors? (Remember)

Since the power amplifiers develop an ac power of the order of few watts and also a large power dissipation at the junctions of transistors used, the transistors used are of large size with large power dissipation rating, called power transistors. Such transistors have heat sinks, a large metal body fit to the transistor to increase the surface area so as to aid the dissipation.

# Classify the power amplifiers. (Remember)

1. According to frequency of operation:
	1. RF power amplifiers ii) AF power amplifiers
2. According to the placement of Q point

1.Class A 2.Class B 3.Class AB 4.Class C

1. Depending on the type of loading
	1. Direct coupled ii) Transformer coupled

# Define efficiency of power amplifiers? (Remember)

Efficiency of a power amplifier is the ratio of output power (ac) to the input power (dc).

%η = Pac / Pdc x 100

# Give the relationship between the power dissipation and operating temperature of a power transistor. (Remember)

When the operating temperature exceeds the highest value at which the maximum permissible power dissipation is rated, the permissible transistor power dissipation decreases linearly with an increase in the operating temperature up to the rated maximum operating temperature.

# What is the use of heat sinks? (Remember)

To avoid thermal runaway, sometimes heat sinks are used providing more surface area for heat dissipation, both by conduction and convection.

# Define class A amplifiers. (Remember)

The power amplifier is said to be a class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

# What is cross over distortion? (Anna Univ Dec 2010) (Remember)

In class B amplifiers the transistor is supposed to operate for a full half cycle of the input. But because of the cut in voltage, the transistor starts conducting only after 0.7V. The distortion caused by this is called cross over distortion.

# What is harmonic distortion? (Remember)

Distortion in the output, caused by the nonlinearity of transistor characteristics is called harmonic distortion. Second harmonic produces the highest distortion.

# What are the advantages of a transformer coupled class A amplifier? (Remember)

1. The efficiency is higher than a direct coupled amplifier.
2. The dc bias current is isolated from the load.
3. Maximum power transfer can be achieved because impedance is matched.

# What is the expression for power dissipation of a power amplifier? (Remember)

Pd = Pdc(input) – Pac (output)

# How can the harmonic distortion be eliminated? (Understand)

By canceling out the second harmonic output. Push – pull circuits accomplish this.

# How is cross over distortion eliminated? (Anna Univ Dec 2010) (Understand)

The basic reason for the cross over distortion is the cut in voltage of the transistor junction. To overcome this cut in voltage, a small forward bias is applied to the transistors.

# Write the condition for maximum power dissipation. (Understand)

Vm = 2 / π VCC

Where Vm = max ac voltage.

# What are the advantages of complementary symmetry class B push-pull amplifiers? (Remember)

1. As the circuit is transformer less, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves due to lack of transformer.

# What do u mean by harmonics? (MAY JUNE 2014) (Remember)

A harmonic is a signal or wave whose [frequency](http://searchcio-midmarket.techtarget.com/definition/frequency) is an integral (whole-number) multiple of the frequency of some reference signal or wave. The term can also refer to the ratio of the frequency of such a signal or wave to the frequency of the reference signal or wave.

# What is conversion efficiency ? (MAY JUNE 2014) (Remember)

Energy conversion efficiency (η) is the [ratio](https://en.wikipedia.org/wiki/Ratio) between the useful output of an [energy](https://en.wikipedia.org/wiki/Energy_conversion_machine) [conversion machine](https://en.wikipedia.org/wiki/Energy_conversion_machine) and the input, in [energy](https://en.wikipedia.org/wiki/Energy) terms.

# What is the effect of millers capacitance on the frequency response of an amplifier. (NOV/DEC2014) (Remember)

The Miller effect accounts for an increase in the equivalent input [capacitance](http://www.answers.com/topic/capacitance) of an inverting voltage [amplifier](http://www.answers.com/topic/amplifier-1) due to amplification of capacitance between the input and output terminals. Although Miller effect normally refers to capacitance, any impedance connected between the input and another node exhibiting high gain can modify the amplifier input impedance via the Miller effect.

This increase in input capacitance is given by



where *AV* is the gain of the amplifier and C is the feedback capacitance. The Miller effect is a special case of Miller's theorem.

# Relate gain and bandwidth of single and multistage amplifier (NOV/DEC2014) (Remember)



1. **The ac schematic of an NMOS common-source stage is shown in the figure. Where part of the biasing circuit has been omitted for simplicity. For the N-Channel MOSFET M1 , the transconductance gm=1 mA/V and body effect and channel length modulation effect are to be neglected. Find the lower cut-off frequency. (APRIL/MAY 2015) (Apply)**



1. **What is the reason for reduction in gain at lower and higher frequencies in case of amplifiers? (Nov-Dec 2016) (Understand)**

Thus the effective voltage input is reduced. The output also reduces. The lower the frequency, the lesser will be the gain. This reduction in gain is due to negative feedback.

As the frequency of the input signal increases, again the gain of the amplifier reduces. Firstly the b of the transistor decreases at higher frequency. Thus reducing the voltage gain of the amplifier at higher frequencies as shown in figure below and The other factor responsible for the reduction in gain at higher frequencies is the presence of various capacitors



# Determine the unity – gain bandwidth of a FET with parameters Cgd = 10fF , Cgs= 50fF and gm = 1.2mA/V (Nov-Dec 2016) (Apply)



1. **Sketch the expanded hybrid pi model of BJT ? (May-June 2016)**



**Part – B**

1. Give the design procedure for heat sinks. (6 marks) **(Anna Univ May 2007)(Remember)**
2. Draw a complementary symmetry power amplifier using BJTs and a dual power supply. Explain its operation. How can it be converted to work with a single supply? Compare the circuits in terms of component counts. **(Analyze)**
3. Write notes on MOSFET power amplifier, Thermal stability and heat sink. (**MAY JUNE 2014) (Remember)**
4. derive fα , fβ and f γ (**NOV/DEC 2014) (Remember)**
5. For the circuit shown find the cut-off frequencies due to C1 and C2 (**NOV/DEC 2014) (Apply)**



1. Explain the high frequency operation of common source amplifier with its equivalent circuit **(NOV/DEC 2014) (Remember)**
2. Derive the expression for cut-off frequency of a BJT. (**NOV/DEC 2016) (Remember)**
3. Construct the high frequency equivalent circuit of a MOSFET from its geometry and derive the expression for short circuit current gain in the common – source configuration. (**NOV/DEC 2016) (Remember)**
4. With neat sketch explain hybrid π CE transistor model. Derive the expression for various components in terms of ‘h’ parameters. **(Remember)**
5. Discuss the frequency response of multistage amplifiers. Calculate the overall upper & lower cutoff frequencies. **(Remember)**
6. Discuss the low frequency response & the high frequency response of an amplifier. Derive its cutoff frequencies. **(Remember)**
7. Discuss the terms rise time and sag. 5. Write short notes on high frequency amplifier. 6. Derive the gain bandwidth for high frequency FET amplifiers. **(Remember)**
8. Derive the expression for the CE short circuit current gain of transistor at high frequency

# (Remember)

1. What is the effect of Cb’e on the input circuit of a BJT amplifier at High frequencies?

# (Understand)

1. Derive the equation for gm which gives the relation between gm, Ic and temperature.

# (Remember)

1. Explain the high frequency analysis of JFET with necessary circuit diagram & gain bandwidth product. **(Remember)**
2. Discuss the frequency response of MOSFET CS amplifier. **(Remember)**
3. Determine the bandwidth of CE amplifier with the following specifications. R1=100kΩ, R2=10kΩ, RC=9kΩ, RE=2kΩ, C1= C2=25µF, CE=50µF, rbb’=100Ω, rb’e=1.1KΩ, hfe=225, Cb’e=3pF and Cb’c=100pF. **(Create)**
4. At Ic=1mA & VCE=10v, a certain transistor data shows Cc=Cb’c=3pF, hfe=200, & ωT=-500M rad/sec. Calculate gm, rb’e, Ce=Cb’e & ωβ **(Create)**
5. Determine the 3 dB frequencies and mid band gain of a cascade circuit. Th parameter V+

= 10 V , V=-10 V RS=0.1K R1 =42.5K , R2= 20.5 K R3=28.3K RE=5.4 K RC= 5K and RL

=10 K CL=0. The transistor parameters are β= 150 , VBE(ON)=0.7V VA= infinity Cπ=35 pF and Cµ=4pF (M**ay-June 2016**)(**Apply)**

1. **The transistor has the** parameter β=125 , VBE(ON)= 0.7 V , VA= 200 Cπ=24 pF and Cµ=3pF calculate miller capacitance , determine the 3db frequency , determine the small signal mid band voltage gain. Where RS=1K R1=20K R2=20K RC=2.3K RE=5K RL=5K

,VCC=±5V (M**ay-June 2016**)(**Apply)**

# ASSIGNMENT

1. Design Class D Amplifier with two push pull transistor switches that approaches 100% efficiency **(Create)**
2. If the ideal push-pull amplifier operates at max dissipation, Show that its efficiency is 50% **(Remember)**
3. Design Class B amplifier with Complimentary symmetry Vcc=15V and load resistance

=10Ω. **(Create)**

1. In a class B amplifier Vce=2V and Vcc=15V. Find Collector circuit efficiency

# (Remember)

**Part A**

1. **Write necessity of a dc power supply in electronic circuits**. **(Remember)**

The dc power supply provides a unipolar voltage. A number of electronic circuits such as amplifiers, oscillators, etc., and appliances such as TV, VCR, etc., operate fully or partly on dc power supply. Hence it is an important device.

# What is a rectifier? What are its types? (Remember)

A rectifier is a device which converts ac voltage to pulsating dc voltage, using one or more p-n junction diodes. The types are half wave rectifier and full wave rectifier.

# What are the important points to be studied while analyzing the various rectifier circuits? (Remember)

* 1. Waveform of the load current
	2. Regulation of the output voltage
	3. Rectifier efficiency
	4. Peak value of current in the rectifier circuit
	5. Peak inverse voltage of the diode
	6. Ripple factor

# Write the expression for rectification efficiency and the values for the same for the rectifiers. (Remember)

Rectification efficiency η = DC output power / AC input power

= PDC / PAC η of HWR = 40.6%

η of FWR = 81.2%

# What are the disadvantages of a HWR? (Remember)

HWR uses only one diode hence the output is obtained for only one half cycle of the input. Hence the theoretical rectification efficiency is only 40.6%. Practical value will still be less.

Also the circuit suffers from dc saturation.

Since the dc current through the load also flows through the secondary winding of the transformer, the core of the transformer experience dc saturation. To minimize the saturation, the transformer size has to be increased accordingly.

This increases the cost. The ripple factor is too high. So the output contains a lot of varying components. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.

# What is voltage regulation? (Remember)

The voltage regulation is the ratio of change in dc output voltage between no load and full load to dc voltage at full load.

# Compare HWR and FWR. (May 2010) (Remember)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | Item | Half-wave | Full-wavecentre tapped | Full-waveBridge |
| 1. | No. of diodes | 1 | 2 | 4 |
| 2. | Peak Inverse voltage ofdiode | Vm | 2Vm | Vm |
| 3. | DC output voltage | 0.318Vm | 0.636Vm | 0.636Vm |
| 4. | Ripple factor | 1.21 | 0.482 | 0.482 |
| 5. | Ripple frequency | fin | 2 fin | 2 fin |
| 6. | TUF | 0.287 | 0.693 | 0.81 |

1. **Write some applications of bridge rectifier. (Remember)**

This is used as a power rectifier circuit for converting ac power to dc power and a rectifying system in rectifier type ac meters such as ac voltmeter.

# Compare center tapped FWR and bridge rectifier circuits. ( May 2012) (Remember)

1. The transformer used in center tapped FWR has three terminals in secondary but in bridge rectifier two terminals in the secondary are sufficient.
2. The peak inverse voltage of each diode in bridge rectifier is Vm whereas in centre tapped FWR is 2 Vm.

# Write the expression for voltage regulation. (Remember)

Voltage regulation = (Vdc) no load – (Vdc) full load / (Vdc) full load.

# Define TUF and rectification efficiency. .( May 2009) (Remember)

TUF may be defined as the ratio of dc power delivered to the load and the ac rating of the transformer secondary. Mathematically, the transformer utilization factor or the TUF is given by

TUF = DC power delivered to the load / AC rating of the transformer secondary

= Pdc / Pac (rated)

Rectification efficiency is defined as the ratio of the dc power delivered to the load to the ac input power from the secondary winding of the transformer. This is given by,

η = DC power delivered to the load / AC input power from the transformer secondary

= Pdc / Pac

# Which filter is used in high current applications? (Remember)

Inductor filter is used in high current applications since its ripple factor reduces with low load resistance.

# What is the advantage of fold back current limiting? (Remember)

This method uses the variation of output voltage and varies the load current accordingly. So if the load resistance decreases, both current and voltage are brought to minimum, so the power consumption by the load is small.

# Explain briefly the term critical inductance. (Remember)

The value of the inductance of the choke filter that makes the diode to conduct the entire 180˚ of the ac supply is called critical inductance.

# List three reasons why an unregulated supply is not good enough for some applications? (Remember)

1. For electronic circuits, and appliances unregulated power supply possess a serious problem because any irregular variation in voltage will prevent proper operation of devices.
2. A surge current or any such increase in current may damage the low current devices.
3. For various load conditions, an unregulated power supply outputs a continuously varying output which decreases the performance of the circuit.

# What is the function of a filter? (Remember)

A filter smoothers out the ripples present in the output of a rectifier and hence produces unregulated dc output.

# Why are protection circuits required for dc power supplies? (Remember)

In dc power supplies short circuiting or overload condition draws a heavy current which damages the devices in series. Hence protection circuits are required.

# List the merits of IC regulators? (Remember)

They are compact, easy to use and provide a fixed voltage. The connections necessary are very less. They provide local regulation in electronics systems that may require several different supply voltages.

# What are the values of PIV for HWR and FWR using ideal diode and sinusoidal input? (Remember)

The PIV for HWR is Vm and that for centre tapped FWR is 2Vm. For a bridge rectifier, it is Vm.

# For a voltage regulator, the output voltage at a load current of 100mA is 6V. The percentage regulation is 30%. Find the no load output voltage. (Apply)

% Regulation = VNL – VFL / VFL x 100

VNL = (Regulation x VFL) / 100 + VFL

= (30 x 6) / 100 + 6

= 7.80

The no load voltage = 7.80V

# What is the frequency of dc signal? (Remember)

0 Hz.

# What is the function of a bleeder resistor? (Remember)

1. It maintains the minimum current necessary for optimum operation of the inductor and hence limits the values of critical inductance.
2. It prevents dangerous shocks and provides safety to the persons handling the equipment, by acting as a discharging path for capacitors.
3. It acts as a preload on the supply and draws a fixed amount of current continuously from the power supply so that the output voltage at no load is reduced and voltage regulation is improved.

# 23. List the disadvantages of Zener regulator? (Remember)

1. The maximum load current ILmax is limited between IZmax and IZmin which is usually of few milliampere.
2. A large amount of power is wasted in the zener diode and the source resistance so that the power output is decreased.
3. The regulation factor and the output resistance are not very low.

# 24. Mention how overload protection is provided in series voltage regulators. (Remember)

Overload protection is provided by current limiting and foldback limiting methods. When the load resistance decreases to a minimum, the current drawn is usually very high. This is limited using current limiting circuitry and thus overload protection is provided.

# 25 What is voltage multiplier? (May 2008) (Remember)

Voltage multiplier circuits have the capable of delivering a DC voltage two or more times the peak value Vm of the applied AC voltage.

# Define Line regulation and Load regulation. (Au-may2012) (Remember)

* 1. Load regulation
	2. The ability of the power supply to maintain the constant DC output voltage for a wide variation in load current is called load regulation.
	3. Line regulation
	4. The ability of the power supply to maintain the constant output voltage for the input supply fluctuations for a constant load is called line regulation.

# Draw the basic building block of linear mode power supply ? (MAY JUNE 2014) (Remember)



1. **What is CLC filter ? (MAY JUNE 2014) (Remember)**

ClC filter. The capacitor-input filter, also called pifilter due to its shape that looks like the Greek letter π is a type of electronic filter . Filter circuits are used to remove unwanted or undesired frequencies from a signal

# Draw a circuit of current source using MOSFET. (NOV/DEC2014) (Remember)



1. **Draw a CMOS amplifier with NMOS driver and PMOS as active load. (NOV/DEC2014) (Remember)**



1. **Compare NMOS amplifier with enhancement , depletion and resistive load. (APRIL/MAY 2015)(Understand)**

Enhancement MOSFET does not conduct at 0 volt, as there is no channel in this type to conduct. Depletion MOSFET conducts at 0 volt. Moreover when positive cut-off gate voltage is applied to depletion MOSFET, hence it is less preferred.

* The depletion MOSFET does not have any kind of leakage currents such as gate oxide and sub threshold type.
* Depletion MOSFET logic operations are opposite to enhancement type of MOSFETs.
* Diffusion current(i.e. sub-threshold leakage current) exists in enhancement MOSFET while depletion MOSFET do not have any diffusion current.

# List out the advantages of CMOS differential amplifier over MOS differential amplifier. (APRIL/MAY 2015) (Remember)

1. **Why active loads are not used with discrete circuits? (Nov-Dec 2016) (Understand)**

In circuit design, an active load is a circuit component made up of active devices, such as [transistors,](https://en.wikipedia.org/wiki/Transistors) intended to present a high [small-signal](https://en.wikipedia.org/wiki/Small-signal) impedance yet not requiring a large DC voltage drop, as would occur if a large resistor were used instead. Such large AC load impedances may be desirable

# Define CMRR. (Nov-Dec 2016) (Remember)

The common-mode rejection ratio (CMRR) of a differential amplifier (or other device) measures the ability of the device to reject common-mode signals, those that appear simultaneously and in-phase on both amplifier inputs. An ideal differential amplifier would have infinite CMRR; this is not achievable in practice

# What Is Current Mirror Circuit? (May-June 2016) (Remember)



1. **Sketch the MOSFET Cascade current source ? (May-June 2016) (Remember)**

**Part – B**

* 1. Draw a MOS current steering circuit with two sink and two source terminals . write the expression for the terminal currents in terms of reference currents. **(NOV/DEC 2014) (Remember)**
	2. Derive gain , input and output impedance of common souce amplifier with NMOS diode connected active load. **(NOV/DEC 2014) (Understand)**
	3. Draw and explain the operation of a simple MOSFET amplifier with active load and derive its voltage gain using small- signal equivalent circuit**(NOV/DEC 2016) (Understand)**
	4. With necessary diagrams, explain the operation of a CMOS differential amplifiers . Using small signal analysis, derive the expression for its voltage gain. **(NOV/DEC 2016) (May June 2016)(Understand)**
	5. Describe the operation of an NMOS amplifier with either an enhancement load, a depletion load, or a PMOS load. **(Understand)**
	6. Explain the basic MOSFET two transistor current circuits and discuss its operation.

# (Remember)

* 1. Draw the MOSFET cascode current source circuit, explain and discuss the advantage of this design. **(Remember)**
	2. Sketch and describe the advantages of a MOSFET cascode current source used with a MOSFET differential amplifier. **(Remember)**
	3. Design a CMOS differential amplifier with an output gain stage to meet a set of specifications. The magnitude of voltage gain of each stage is to be at least 600. Bias currents are to be IQ=IREF=100µA, and biasing of the circuit is to be V+ =2.5 v and V-

=2.5 v. **(Create)**

* 1. Explain CMOS differential amplifier and derive CMRR. **(Remember)**
	2. Draw a Widlar current source and explain the operation. **(Remember)**
	3. Describe the operation of a PMOS amplifier with an enhancement load, a depletion load.

# (Remember)

* 1. Explain the CMOS common source and source follower with neat diagram. **(Remember)**

# ASSIGNMENT

1. Design a Zener voltage regulator to meet output voltage =5V, load current =10mA,Zener wattage=400mW and input voltage=10+\_2V **(Create)**
2. A FWR voltage of 18V peak is applied across a 500µF filter capacitor. Calculate the ripple and d.c voltages if the load takes a current of 100mA **(Remember)**
3. In a Zener regulator d.c input is 10V+\_20%. The output requirements are 5V,20mA. Assume and as 5mA and 80mA. Design zener regulator **(Create)**
4. A system needs to be powered with 9V d.c source of max current 100mA. Design a circuit to supply power with the available domestic a.c line. Assume any data required but reasonable. Provide short circuit protection**. (Create)**